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Breakdown Effects on MOS Varactors and VCO's

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Abstract: **The gate oxide breakdown effects of deep sub-micron devices, which degrade the performance of MOS varactors that in turn degrade the performance of LC Voltage Controlled Oscillators (VCO's), are presented. On wafer 0.16 μm CMOS devices are stressed; experimental data are analyzed and used for analytical derivations and simulations to show that the breakdown has twofold effects on the performance of the VCO's. Firstly, the increased conductance of the varactor degrades its quality, which increases the phase noise of the VCO's. This also reduces the amplitude at the output of the oscillator. Secondly, the value of the capacitance of the MOS varactor reduces, which shifts the oscillation frequency of the VCO's.**

I. Introduction

The implementation of cheap and reliable monolithic VCO's for the integrated RF CMOS transceivers still remains challenging. Secondary effects of deep sub-micron devices complicate the issue even further. As CMOS device size shrinks, channel electric field becomes higher and hot carrier effects become significant. On the other hand, the gate oxide also becomes ultra thin. When a high gate voltage sustains across the thin gate oxide of a transistor for prolonged amount of time, it often exhibits a phenomenon, which is known as soft and hard breakdown (BD) in the literature. Despite several efforts [1-2], the full understanding of physics behind this phenomenon and its effects on CMOS analog and RF circuits are still subject to further research. This work is the first attempt to analyze and characterize the effects of breakdown on MOS varactors and corresponding effects on LC VCO's. While hot carrier and gate oxide breakdown degrade active devices of the VCO's as well, this work only focuses on the breakdown effects on the MOS varactors.

Variable capacitor is an essential element for designing LC VCO's. The use of MOS transistors to implement varactors has become of increased interest recently [3-4]. While the drain (D) and source (S) are connected, the capacitance between D-S and the gate (G) depends on applied voltage for a certain range. If very high gate voltage persists for prolonged amount of time, which may be the case for VCO circuits, carriers are trapped in the oxide layer. Repeated soft breakdown also changes the profile of the oxide. As a result, the capacitance between G and D-S changes, which in turn shifts the resonance frequency of the LC tank. On the other hand, after the transistors are stressed, measured gate current increases. This can be explained by increased conductance between G and D-S terminal. Thus, the quality of the capacitance degrades, which degrade the phase noise of the VCO. The amplitude of oscillation also decreases, which reduces the effective capacitance across the varactor. This decrease in capacitance shifts and reduces the tuning range of the VCO.

The experimental and measurement setup has been described in section II. In section III, effects of breakdown on MOS devices are presented. The effects of device degradation due to gate oxide breakdown on MOS varactors and thus LC VCO's are analyzed and simulation results are given in section IV. Finally, conclusions are given in section V.

II. Experiments and Measurements

0.16 μm CMOS devices with channel length L = 0.16 μm and channel width W = 10 μm are used in this work. The oxide thickness (t_{ox}) for these devices is 24 Å. Nominal voltage of operation is 1.5 V. On wafer NMOS devices are electrically stressed, tested and measured using Cascode probe station, Agilent 4156B Precision Semiconductor Analyzer, and Agilent 8510C Network Analyzer.

To predict the parameter degradation due to aging, an accelerated aging is modeled through electrical overstress of the devices. A gate voltage V_g = 4.5 V is applied to evaluate the effect of gate oxide breakdown. During experiments, the stress automatically stops to avoid further damage to the oxide when the gate current meets a threshold of 1 mA. Gate current before and after the stress is recorded. S-parameters of the transistors are measured and the BSIM3V3 model is extracted. Once the transistors are stressed, all parameters are obtained with normal bias conditions.

III. Effects of Breakdown on MOS Devices

After the transistors are stressed, measured gate current has been found to be increased. A comparison between fresh and stressed I_g-V_g curves, as shown in Fig.1, confirms the occurrence of this increased gate current due to gate oxide breakdown. The increased gate current can be explained by increased conductance between G and D-S terminal.

A typical transistor small signal model, which assumes a very low (close to zero) conductance from G to D-S, does not hold for the deep sub-micron devices under prolonged operation. A modification is necessary to include the finite conductance for better estimation of RF circuit performance. A modified transistor model is given in Fig. 2.

Measured S-parameters before and after gate oxide breakdown are displayed as solid and dotted lines in Fig. 3 for the frequency range of 50 MHz to 2.3 GHz. It is clear from Fig.3 that S-parameters degrade significantly due to

breakdown effects. After breakdown either a gate-to-channel or a gate-to-extension resistive path is formed. This leads to the change of the input impedance at the gate as evidenced by S11; another connection between the gate and the drain other than the original capacitive path explains the significant degradation of S12; and the change of the reflected impedance at the drain is related to change of S22. The degradation of S21 is consistent with the decrease of g_m.

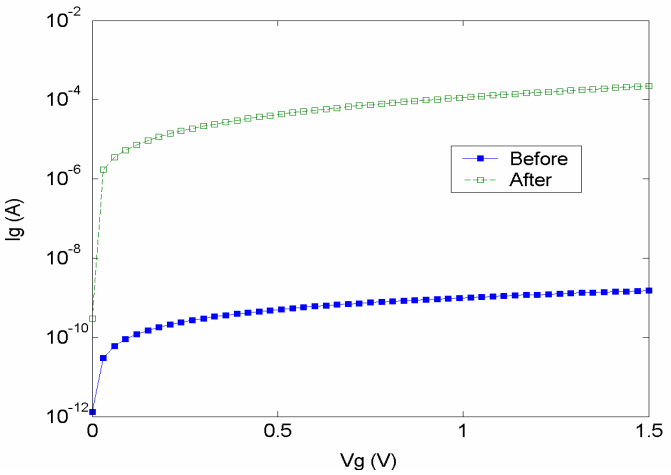

Fig. 1: Ig - Vg characteristics before and after device breakdown

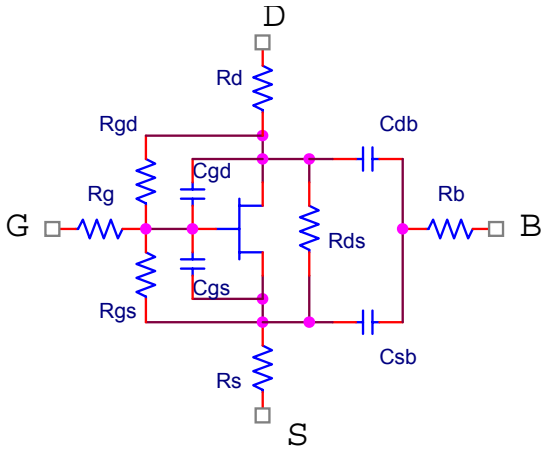

Fig. 2: Equivalent RF transistor model after gate-oxide breakdown

The S-parameters are used to calculate the Y11 as in (1). Input capacitance of the MOS device can be calculated by (2), when D-S are connected which is the case for MOS varactor. Here, f is the frequency of oscillation.

$$Y_{11} = \frac{(1-S_{11})\cdot(1+S_{22})+S_{12}S_{21}}{(1+S_{11})\cdot(1+S_{22})-S_{12}S_{21}} \quad (1)$$

$$C = \frac{\mathrm{Im}(Y_{11})}{2\pi f} \quad (2)$$

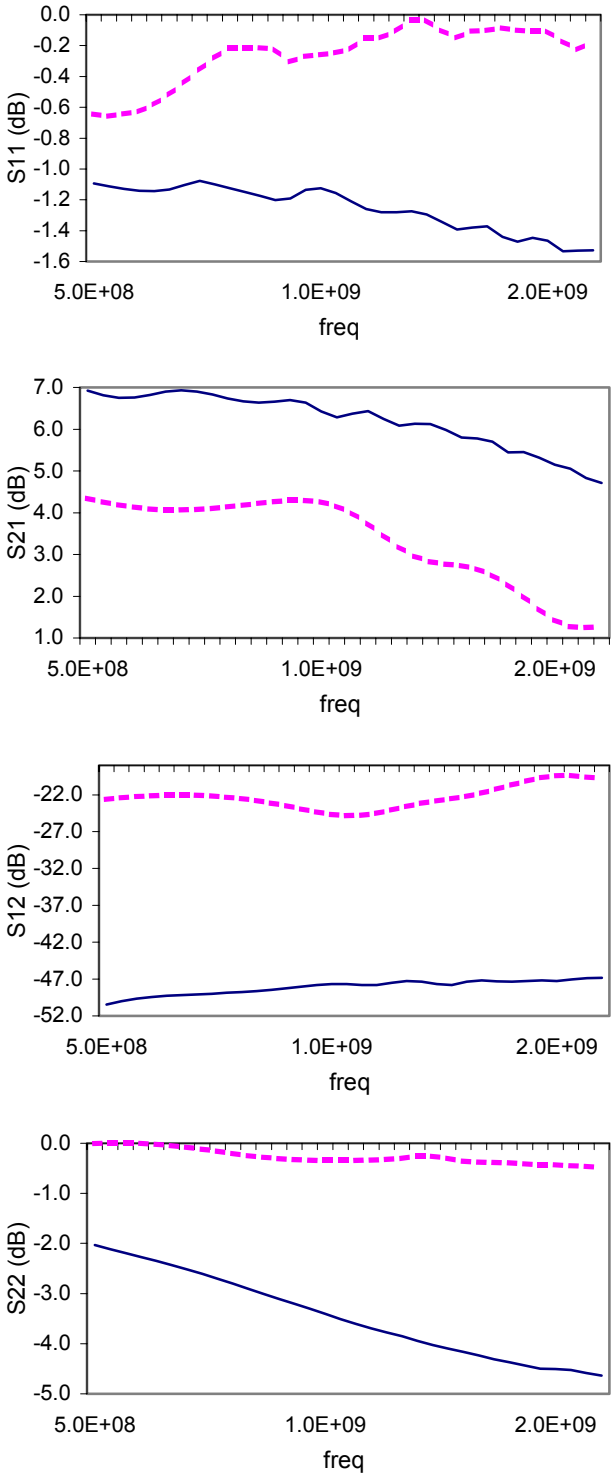

Fig. 3: S-parameters degrade after device breakdown (solid lines: fresh measurement, dotted lines: post-BD measurement

IV. Effcts on MOS Varactors and LC VCO's

A simplified schematic of the LC VCO that has been used for simulation in this work is shown in Fig. 4. Cadence SpectreRF simulator is used to perform the circuit simulation.

The simulation results show that the LC VCO continues to perform with its functionality even after the gate oxide breakdown, but the various performances degrade.

The oscillation frequency of the oscillator is 1.75 GHz. The inductors (8 nH each) are assumed to have quality of 10. Two MOS varactor serve as the capacitors. The control voltage determines the value of the capacitance that determines the frequency of oscillation of the VCO.

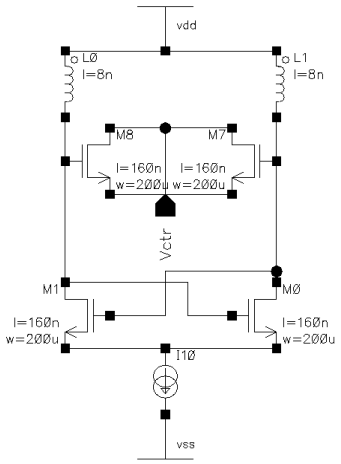

Fig. 4: LC VCO

While the D and S of the varactor are connected, the B is connected to ground. The variable capacitance is formed by G and D-S, which is controlled by the potential of D-S terminal. Device sizes for the varactors are 200/0.16 µm. Number of fingers for the varactor transistors is assumed to be 20 (since the width of the measured NMOS transistors are 10µm).

It has been postulated that due to aging not all fingers of the varactor transistor will undergo soft or hard breakdown. The simulation is performed using varactors with fresh transistor, and with 2, 4, 6, and 10 fingers with breakdown. A parallel conductance (through Ig – Vg measurement) is assumed for the breakdown model of the varactor during simulation.

In order to model the LC tank, let us assume that Rs is the resistance for the finite quality factor of the inductor and m is the number of finger for the MOS varactor of which n fingers undergo breakdown. Let us also assume, R is the resistance parallel to the finger of the MOS varactor transistor that experiences breakdown. R_{gd} and R_{gs} of the fresh transistors are assumed infinity. As such, the LC tank can be modeled as Fig. 5(a). Through impedance transformation the equivalent parallel resistance for the inductance $(2L_s)$ is $\frac{2\omega^2 L_s^2}{R_s}$ and equivalent parallel resistance for the capacitance $\left(\frac{1}{2}mC_g\right)$ is $\frac{2R}{n}$. A narrow band of interest is assumed for these transformations. The equivalent tank is shown in Fig. 5(b). Thus, the equivalent parallel resistance of the tank is:

$$R_{eq} = \frac{2\omega^2 L_s^2 R}{n\omega^2 L_s^2 + RR_s} \tag{3}$$

When breakdown happens to any of the fingers of the MOS varactor transistor the oscillator does not operate in the voltage limited region. To determine the amplitude of oscillation, it can be assumed that the diffrential pair is a current source switching between I_0 (tail current) and $-I_0$ parallel with RLC tank. At resonance frequency, admittances of L and C cancel leaving R_{eq} [5]. As a result, the amplitude of the oscillator is limited by the current source and that can be expressed in terms of the tail current and the equivalent parallel resistance of the LC tank.

$$V_m = I_o R_{eq} \tag{4}$$

To obtain the estimated amplitude due to finite conductance of the varactor let us substitute R_{eq} from (3):

$$V_m = \frac{2I_0\omega^2 L_s^2 R}{n\omega^2 L_s^2 + RR_s} \tag{5}$$

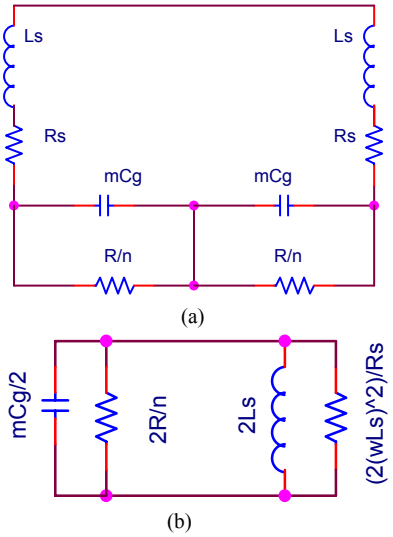

Fig. 5: (a) LC tank (b) Equivalent circuit

As the gate oxide breakdown effects become serious with increased number of fingers that undergo breakdown, the equivalent parallel resistance for the MOS varactor decreases, and, as a result, the amplitude of oscillation reduces according to (5). This has been also observed through simulation of the VCO and tabulated in Table I. Decreased amplitude of the oscillator may not be sufficient for proper operation of the subsequent circuits.

The phase noise of the oscillator can be expressed by the Leeson's proportionality [6]:

$$\Im(\omega_m) = \frac{1}{V_m{}^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{Q} \cdot \frac{1}{\omega_m{}^2} \cdot \qquad (6)$$

As the amplitude of the oscillation decreases due to the gate oxide breakdown, the phase noise of the signal increases according to (6). This can be seen in Table I and Fig. 6.

TABLE I
EFFECTS OF INCREASED GATE CONDUCTANCE ON OSCILLATOR PERFORMANCE (FROM SIMULATION)

Number of fingers Breakdown	Freq. of oscillation (GHz)	Phase Noise @ 100 KHz (dBc)	Amplitude (V)
Fresh	1.75	-106.9	1.53
2	1.86	-101.6	1.07
4	1.96	-98.0	0.82
6	2.03	-96.6	0.66
10	2.05	91.6	0.45

Another effect of decrease in amplitude due to gate oxide breakdown is on the capacitance value of the varactor. Due to decreased value of the amplitude of oscillation, varactor experiences less amount of voltage swing across it. Since, the C-V curve across a varactor is nonlinear and at high voltage swing, it exhibits more capacitance [3,7]. As a result, the average value of the capacitance reduces after breakdown. The decrease of the capacitance value increases the frequency of oscillation according to (7). The simulation of the VCO verifies that fact, which is shown in Table I.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \qquad (7)$$

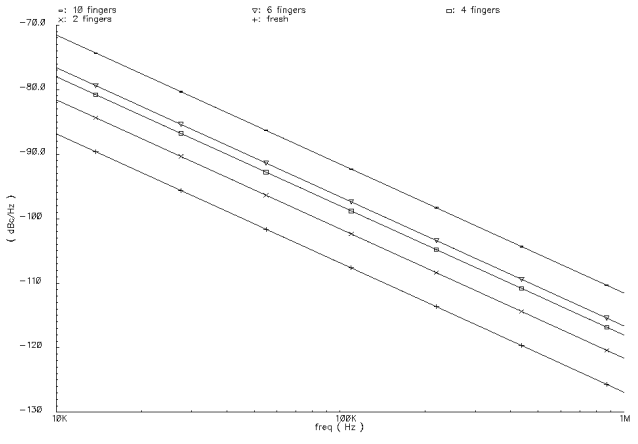

Fig. 6: Phase noise of the oscillator with different numbers of fingers breakdown

The capacitance between G and D-S, which is found through S parameter measurements, decreases after gate oxide breakdown. The degradation of the capacitance is shown in Fig. 7 for the frequency range of 500 MHz to 2.3 GHz.

The effect of decreased amplitude on capacitance reduction and the capacitance reduction due to capacitance profile change across the oxide and channel both work in the same direction, and according to (5) both phenomena increase the frequency of oscillation. As a result, the VCO's tuning range will shift and reduce.

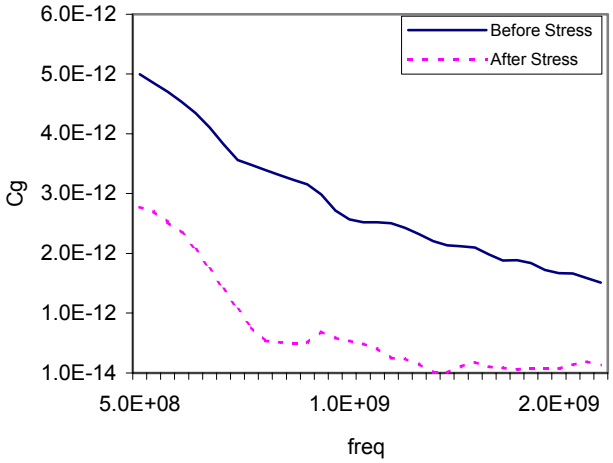

Fig. 7: Degradation of the varactor capacitance after gate oxide breakdown

V. CONCLUSION

Gate oxide breakdown effects on MOS varactors are presented. It has twofold effects on varactors; it increases the conductance and decreases the capacitance. The effects of such degradation on LC VCO's are argued through analytical equations and simulation results. It has been shown that amplitude of oscillation decreases, phase noise increases and frequency of oscillation drifts. Thus, gate oxide breakdown raises a serious reliability issue.

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